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HARDWARE

The New AP5 User Guide

What is the AP5?

The **AP5** is an interface card for the Acorn Electron that is fitted with either a Plus 1 or Slogger ROMBox 2 fitted. It provides the following features:

- BBC compatible* Tube interface
- BBC compatible* 1MHz interface
- 2 x User Ports with one of them BBC compatible*
- 3 x configurable IC sockets
- I^2C Interface
- Serial Interface

The 3 x configurable IC sockets are described, in detail, later in this User Guide.

* Note 1: There are some slight differences between the BBC/Master and the Electron **AP5** interfaces. See the relevant sections, for these differences.

CONTENTS

What is the AP5? ---------- Inside Front cover

1 Using the AP5

Plugging the AP5 into a Cartridge Slot ---------- 2

2 Interface Connectors

Tube Interface ---------- 3
1MHz BUS Interface ---------- 4
BBC Compatible User Port Interface ---------- 5
The Second User Port Interface ---------- 5
EUPURS Serial Connector ---------- 6
I²C Connector ---------- 7

3 The IC Sockets

ROM13 ---------- 8
ROM0/2 ---------- 8
ROM1/3 ---------- 8
Write Protection ---------- 9

4 Jumpers

J1 & J2 ---------- 10
Mode 0 ---------- 10
Mode 1 ---------- 10
Mode 2 ---------- 10
Mode 3 ---------- 10
J3 ---------- 13
J4 & J5 ---------- 13

5 Technical

Access to the XC9572 spare pins ---------- 13
External power connector (J6) ---------- 13
Schematic (fold-out) ---------- 14

1 Using the AP5

Plugging the AP5 into a Cartridge Slot:

The **AP5** is designed to work with an Acorn Electron that is fitted with an Acorn/P.R.E.S. Plus 1 or slogger ROMBox 2.

The **AP5** is a standard format Acorn Cartridge and will work in either of the two Cartridge Slots.

Important: Install the **AP5**, into either one of the cartridge slots, **before turning on the power to the Electron!**

Note: The **AP5** is **NOT** BBC Master compatible!

You will need to read the sections on IC Sockets, Modes and Jumpers before you fit any ICs. If you ordered a ready built **AP5** it will have been shipped to you with none of the Jumpers fitted. This sets the **AP5** to the default **Mode 0** allowing RAM (62256), EEPROM (28C256) and EPROM (27128 or 27256) to be fitted. These parts can be supplied by Retro Hardware, if required. The eMail address, for Retro Hardware, can be found on the back page of this User Guide.

2 Interface Connectors

Tube Interface:

The **AP5** Tube interface (SK1 – the 40 Way connector) is compatible with all 2nd Co-Processors that are designed to work with the BBC, BBC+ and Master Computers.

You will need to have a copy of the Tube Interface software, in ROM, installed for this interface to work correctly. This can be a ROM fitted into any of the Electrons Sideways ROM banks. However, the Tube code is already embedded into the New Plus 1 Utility ROM. This was originally developed for the **AP6**, however, there's a cut-down version available as a replacement for the Plus 1 ROM. The standalone ROM or replacement Plus 1 ROM is obtainable from Retro Hardware, who's eMail address can be found on the back page of this User Guide.

Further details of the Tube interface can be found in the BBC's or Master's Advanced User Guide.

For the Tube interface connections, see the Schematic on Page 14.

The Electron Tube Interface is mapped to:
FRED addresses &E0-&EF (&FCB0-&FCBF)

1MHz BUS Interface:

The **AP5** 1MHz BUS interface (SK2 – the 34-way connector) is largely compatible with the BBC 1MHz BUS, however, unlike the BBC/Master, FRED is not fully available. The following is a list of FRED address that are available, showing some allocations:

&FC00-&FC03	Byte-Wide Expansion RAM
&FC08-&FC0F	Ample M2000 MIDI Interface (see also FCF0)
&FC18-&FC1F	Reserved for use by Acorn
&FC20-&FC27	IEEE Interface
&FC28-&FC2F	Electron Econet
&FC30-&FC3F	Reserved for use by Acorn
&FC40-&FC4F	Hard Drive Access
&FC80-&FC8F	Test Hardware
&FCA0-&FCAF	
&FCF0-&FCF7	JGH/ETI MIDI Control (see also FC08)

DataCentre:

&FCF8 VNC1L	Data Port	
&FCF9 VNC1L	Control Port	
&FCFA NVRAM	Data Port	
&FCFB NVRAM	Data Direction Register	
&FCFC NVRAM	Clock	*Clash with AQR Paging Register*
&FCFD NVRAM	Write Protect	*Clash with AQR Unlock*
&FCFE Page RAM MSB		*Clash with AQR Lock*
&FCFF Paged RAM LSB		

Note: Some of the above allocations may not have been used on the Electron! Some others e.g., Acorn allocated, would now be free to use.

BBC Compatible User Port:

This is User Port 1 interface (SK3 – 20-way connector).

Please see the BBC/Master Advanced User Guide for full programming details of this port.

The BBC/Master User Port is mapped to:
SHELA addresses &60-&6F - &FE60-&FE6F – Port B

The Electron User Port 1 is mapped to:
FRED addresses &B0-&BF - &FCB0-&FCBF – Port B

The Second User Port Interface:

This is User Port 2 interface (SK4 – 20-way connector).

Please see the BBC/Master Advanced User Guide for full programming details of this port.

The Electron User Port 2 is mapped to:
FRED addresses &B0-&BF - &FCB0-&FCBF – Port A

There is no equivalent second User Port available on the BBC/Master, as Port A is used for the Printer output.

EUPURS Serial Connector:

This is a 7 way 2.54mm (0.1") header for connection to a serial lead (PL1). The interface is driven from the User Port 2 VIA and requires software, on ROM, to drive it – See below for details.

The connections:

Pin #	Pin name	'D' Pin function	'D' Pin #
1	PA0	RXD	2
2	PA1	RTS	7
3	PA6	CTS	8
4	PA7	TXD	3
5	LK*	DTR	4
6	LK*	DSR	6
7	Gnd	Gnd	5

* Pin 5 & 6 are linked on the AP5 PCB.

Note: The standard BBC UPURS cable has the resistor/diode protection built into it and is therefore not suitable for the Electron UPURS. Suitable cables and FTDI (serial to USB interface) are available from Retro Hardware*.

The Project:

UPURS - Fast serial transfer utilities for the BBC Micro - by Martin Barr

Link to full details: www.retro-kit.co.uk/UPURS/

The UPURS ROM and User Guide is available for download from the above link (use the Electron version!). A ROM and printed User Guide is available from Retro Hardware*.

* The Retro Hardware eMail address can be found on the back page of this User Guide.

I²C Connector:

This is a 4 way 2.54mm (0.1") header for connection to your I²C projects (PL2). The interface is driven from the User Port 1 VIA and requires software, on ROM, to drive it – See below for details.

The connections:

Pin #	Pin name	I²C Pin name
1	+5V	+5V
2	PB0	SDA
3	CB2	SCL
4	Gnd	Gnd

A suitable cable, connector to wire ended (specify length when ordering), is available from Retro Hardware*.

The Project:

I²C (Inter-Integrated Circuit) - "I2C 4 U" for the Electron - by Martin Barr.

Link to full details:

http://stardot.org.uk/forums/viewtopic.php?f=3&t=10966&p=135632 - p135596

The ROM is available for download from the above link. A ROM is also available from Retro Hardware*.

* The Retro Hardware eMail address can be found on the back page of this User Guide.

3 The IC Sockets

ROM13 - The Left had side 28 pin ROM socket.

This socket is mapped to ROM position 13 and is considered High Priority e.g. The Operating System will 'see' this position before lower numbered ROMs.

If you have another ROM 13 e.g., in another cartridge, AP6, ROMBox 2 or GoSDC etc., you can disable the socket in the **AP5** by fitting **J3** – See section 4 - **Jumpers**.

Note: Currently, none of the jumpers affect this socket.

ROM13 mapping

Normal/32K	Device:	32K ROM/RAM	
	ROM13 A:	0000-3FFF	(bank A)
	ROM13 B:	4000-7FFF	(bank B)

ROM13 will accept either 16K or 32K EPROM, 32K EEPROM or 32K RAM.

Bank switching is available for 32K parts. The mapping, above, shows that the lower half of the device is mapped to the default bank A.

ROM0/2 - The Centre 28 pin ROM socket.

This socket is mapped dependant on which cartridge socket it is in.

Fitted into the cartridge socket nearest the keyboard, this ROM will be mapped as ROM position 0.

Fitted into the cartridge socket furthest from the keyboard, this ROM will be mapped as ROM position 2.

ROM1/3 - The Right Hand 28 pin ROM socket.

This socket is mapped dependant on which cartridge socket it is in.

Fitted into the cartridge socket nearest the keyboard, this ROM will be mapped as ROM position 1.

Fitted into the cartridge socket furthest from the keyboard, this ROM will be mapped as ROM position 3.

For the full use of IC sockets 0/2 & 1/3 see section 4 - **Jumpers.**

Write Protection:

All 3 IC sockets, by default, have Write Protection. This is accessed by writing to &FCDA, &FCDB, &FCDC, &FCDD, &FCDE or &FCDF as follows:

A write to:

&FCDA - Unlock	ROM13*	Enable Writes.
&FCDB - Lock	ROM13*	Disable writes – Default on reset.
&FCDC - Unlock	ROM0/2	Enable Writes.
&FCDD - Lock	ROM0/2	Disable writes – Default on reset.
&FCDE - Unlock	ROM1/3	Enable Writes.
&FCDF - Lock	ROM1/3	Disable writes – Default on reset.

* Unlocking/Locking ROM13 will also affect ROM position 15, if you have AP6 fitted!

*LOCK and *UNLOCK are commands that are supported by the following ROMs: AP6 and the Retro Hardware replacement Plus 1 ROM.

These and other ROMs are available from Retro Hardware – see back page of this User Guide for the eMail address.

See also J4 & J5 in section 4 – **Jumpers**.

4 Jumpers

J1 & J2

Together these 2 jumpers control 4 different modes for IC sockets ROM0/2 and ROM1/3, as follows:

Mode 0 - J1 & J2 not fitted

Normal/32K	Device:	32K ROM/RAM	32K ROM/RAM	
	ROM0/2 A:	0000-3FFF		(bank A)
	ROM0/2 B:	4000-7FFF		(bank B)
	ROM1/3 A:		0000-3FFF	(bank A)
	ROM1/3 B:		4000-7FFF	(bank B)

Mode 1 - J1 fitted J2 not fitted

Normal/64K	Device:	empty	32K ROM or 64K ROM		
	ROM0/2 A:		0000-3FFF	4000-7FFF	(bank A)
	ROM0/2 B:		(unmapped)	0000-3FFF	(bank B)
	ROM1/3 A:		4000-7FFF	C000-FFFF	(bank A)
	ROM1/3 B:		(unmapped)	8000-BFFF	(bank B)

Mode 2 - J1 not fitted J2 fitted

MMFS/32-64K	Device:	16K RAM	32K ROM or 64K ROM		
	ROM0/2 A:	3600-3FFF	0000-35FF	4000-75FF	(bank A)
	ROM0/2 B:	3600-3FFF	(unmapped)	0000-35FF	(bank B)
	ROM1/3 A:		4000-7FFF	C000-FFFF	(bank A)
	ROM1/3 B:		(unmapped)	8000-BFFF	(bank B)

Mode 3 - J1 and J2 fitted

ADFS/32-64K	Device:	16K RAM	32K ROM or 64K ROM		
	ROM0/2 A:	3000-3FFF	0000-2FFF	4000-6FFF	(bank A)
	ROM0/2 B:	3000-3FFF	(unmapped)	0000-2FFF	(bank B)
	ROM1/3 A:		4000-7FFF	C000-FFFF	(bank A)
	ROM1/3 B:		(unmapped)	8000-BFFF	(bank B)

Terminology:

Mode: This is the title for the scheme, as described immediately below, and is followed by which jumpers are fitted for that Mode.

Device: This row shows the header for the type of memory fitted and its mapping below.

ROM0/2:
ROM1/3: Indicates which IC socket is being described and is dependant on which cartridge slot it is in.

Bank: All 3 IC sockets can accept several device types and sizes (Mode dependant!) e.g. **(1)** EPROM 27(C)128, 27(C)256 and 27(C)512 **(2)** EEPROM 28C256 **(3)** RAM 62256. Further, each visible 16K block can be 'banked' e.g. Take ROM0/2 IC socket containing a 27(C)256 EPROM. The ROM position 0 or 1

(dependant on which cartridge socket it was in) would only show 16K. However, there is a mechanism (described below) to switch from the lower addressed 16K to the upper addressed 16K. This allows programs/utilities to hold twice the amount of code. There were a number of these ROMs supplied by companies such as Computer Concepts, Watford Electronics and P.R.E.S. They all relied on a programmable device, on a carrier board, to carry out the bank switching. The **AP5** has implemented this switching within the on-board CPLD, however, it will require some changes to existing code to work with the different switching mechanism in the **AP5**.

Bank Switching:

To switch between the 16K banks it is necessary to write the value &96 or &97 to location &AFFF three times! Writing &96 sets the default bank (this bank is the default after a reset) – writing &97 will select the second bank. Bank switching is now supported with version 1.31 of the AP6/Plus 1 support ROM.

Or, use the command SRPAGE which has been added to the Plus 1and AP6 support ROMs.

Mode 0:

This Mode will accept either 16K or 32K EPROM, 32K EEPROM or 32K RAM in either ROM0/2 or ROM1/3 sockets.

Note 1: You will not have access to the full capacity of parts over 16K!

Bank switching is available for 32K parts. **Fig. 1** shows that the lower half of the device is mapped to the default bank A for each socket.

Mode 1:

This mode will accept 16K*, 32K or 64K EPROM or EEPROM.

Note: The memory should be fitted into ROM1/3 IC socket. ROM0/2 IC socket is **NOT** supported in this Mode!

Using a 32K part will give 2 x 16K (ROM position 0/2 & 1/3), with no bank switching. See **Fig. 1** for the address mapping.

Using a 64K part will give 2 x 16K (ROM position 0/2 & 1/3), with bank switching. See **Fig. 1** for the address mapping, noting in particular that bank A, for both positions, are mapped in the upper half of each 32K block. Understand this fully before you program any EPROM externally!

* Using a 16K part: This will be visible in both ROM positions - 0/2 & 1/3.

Mode 2:

This Mode has been implemented specifically to support MMFS E00. See the MMFS User Guide for further details.

The MMFS will run, without changing Page, using RAM (62256) that is fitted into the ROM0/2 socket and either a 32K or 64K EPROM fitted into ROM1/3 socket.

Note the mapping in **Fig. 1**!

With a 32K device fitted: Mapping for ROM position 0/2 is allocated to MMFS. This has ROM available from &0000 to &35FF and RAM available from &3600 to &3FFF. Mapping for ROM position 1/3 is the full 16K of ROM and is mapped to &4000 to &7FFF. Note: No bank switching is available with a 32K device.

With a 64K device fitted: Mapping is slightly different - ROM position 0/2 is allocated to MMFS with ROM available, for bank A, from &4000 to &75FF and bank B from &0000 to &35FF - RAM is available from &3600 to &3FFF with either bank switched-in. Mapping for ROM/1/3 socket is the full 32K – bank A from &C000 to &FFFF and bank B from &8000 to &BFFF.

Mode 3:

This mode is similar to Mode 2 but is designed for ADFS E00. The Mapping for both RAM and ROM, are as follows:

With a 32K device fitted: Mapping for ROM position 0/2 is allocated to ADFS. This has ROM available from &0000 to &2FFF and RAM available from &3000 to &3FFF. Mapping for ROM position 1/3 is the full 16K of ROM and is mapped to &4000 to &7FFF. Note: No bank switching is available with a 32K device.

With a 64K device fitted: Mapping is slightly different - ROM position 0/2 is allocated to ADFS with ROM available, for bank A, from &4000 to &6FFF and bank B from &0000 to &2FFF - RAM is available from &3000 to &3FFF with either bank switched-in. Mapping for ROM/1/3 socket is the full 32K – bank A from &C000 to &FFFF and bank B from &8000 to &BFFF.

J3:

Disables ROM 13 when fitted.

J4 & J5:

J4 disables write protection for ROM0/2 in Mode 0 or Mode 1.

J5 disables write protection for ROM1/3 in Mode 0 or Mode 1.

5 Technical

The **AP5** PCB has been designed with access to 6 spare CPLD pins. These are brought out to vias (holes) so that wires can be attached for possible experimentation or modification to the functionality.

Spare1 – pin 39
Spare2 – pin 41
Spare3 – pin 65
Spare4 – pin 66
Spare5 – pin 81
Spare6 – pin 82

External power connector - J6 provides **+5V** and **Gnd.** for powering external circuits.

Primarily for the BeeBSCSI (SCSI emulation*), however, other circuits may be attached – **Caveat:** Maximum current should be limited to 100mA.

* See here for details: https://www.domesday86.com/?page_id=689

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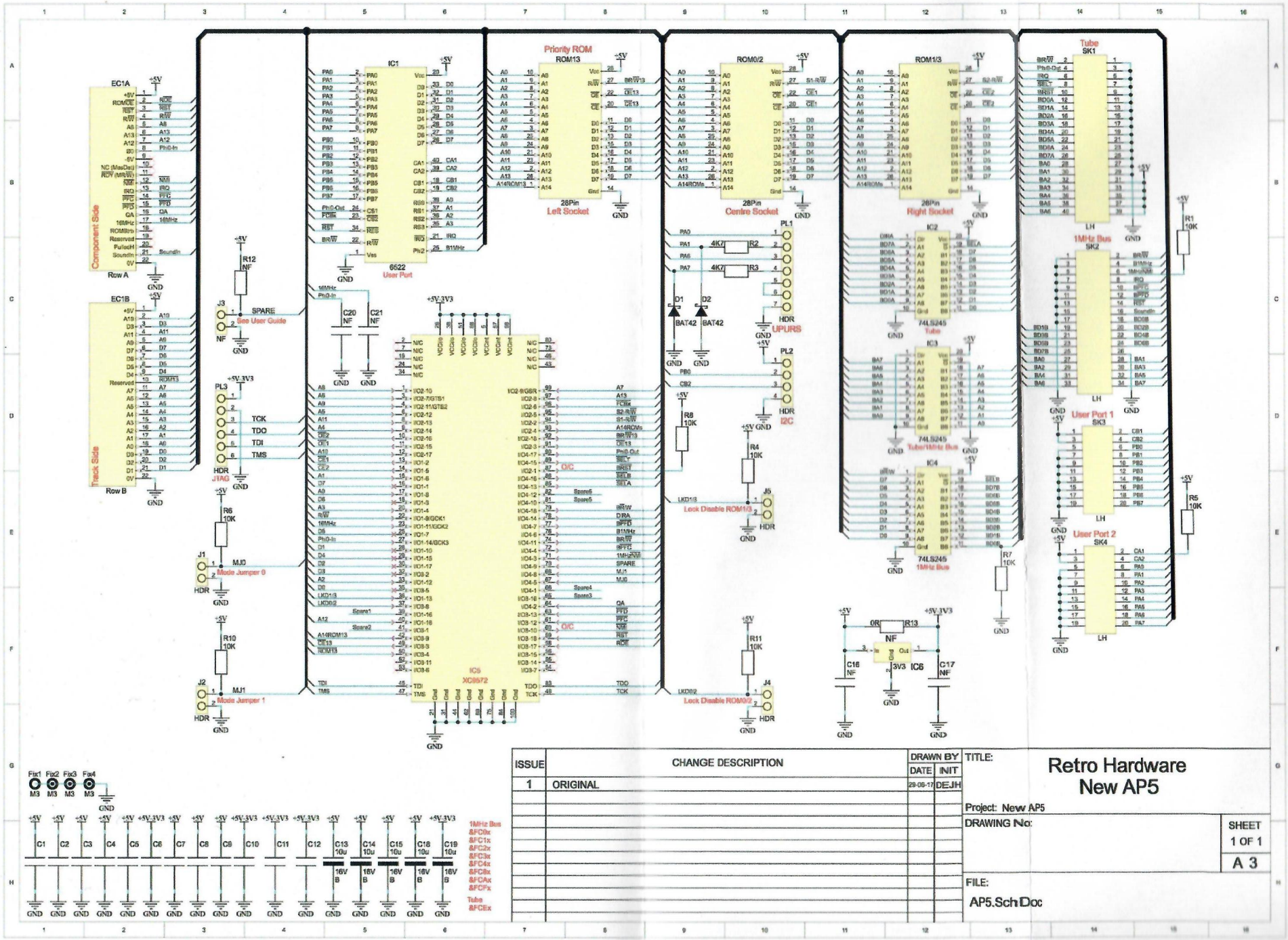

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